added; as a result, claims 36-39, 59-69, and 75-83 are pending in this application. Please note that claims 70-74 were canceled in the last Office Action Response, filed May 4, 2001.

Double Patenting Rejection

In §4 of the Office Action, claim 66 was provisionally rejected under the judicially created doctrine of double patenting over claims 51, 59, 63, 64, and 67 of co-pending Application No. 08/984,561, which has not yet received any final indication of allowed claims. The Applicant requests that the claims of the instant patent application be allowed to issue without a Terminal Disclaimer, and that the issued claims of the instant application be compared to the claims of the cited co-pending application to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Applicant will submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon closing prosecution on the merits for the co-pending application, as needed, or in the alternative, upon receiving an indication of allowance for the relevant claims in the instant application.

§112 Rejection of the Claims

Claims 78 and 83 were rejected in § 5 of the Office Action under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. The Office Action notes that there appears to be no support for "subsequently switching from the pipelined mode of operation to the burst mode of operation." The Applicant appreciates the Examiner's concern, and directs attention to the original application, Figs. 9-12, as well as to the text on page 33, line 17, wherein the statement is made that "The present invention provides switching between burst access, and non-burst access or pipelined modes of operation without ceasing ("on-the-fly"). No WCBR cycle is needed with burst/pipelined mode switching during operation." Also, on page 38, line 12, "Moreover, this type of switching may be accomplished on either read or write cycles, *e.g.*, from a burst EDO read cycle to a pipelined EDO read cycle *and vice-versa*, or from a burst EDO write cycle to a pipelined EDO write cycle *and vice-versa*.". The Applicant submits that these statements, along with numerous others in the original application, are sufficient to support

"subsequently switching from the pipelined mode of operation to the burst mode of operation" as an element of claims 78 and 83, and therefore respectfully requests that this objection be withdrawn.

§102 Rejection of the Claims

Claims 36-39, 59-62, and 75-83 were rejected in § 7 of the Office Action under 35 USC § 102(e) as being anticipated by Manning (U.S. Patent No. 5,610,864). However, the MPEP requires that "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131. Thus, the Applicant asserts that the Office has failed to show that Manning discusses the identical invention claimed in the instant application, and respectfully traverses the rejection by the Office.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in another Office Action mailed to the Applicant on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support *choosing, switching* or *selecting* between burst and *pipelined* modes of operation (especially using a mode select signal), as claimed in claims 36-39, 59-62, 63-69, and 75-83? The Applicant also respectfully draws attention to a statement in the instant Office Action (see § 9) that Manning discloses the limitation of "selecting between a burst mode and a pipeline modes of operations", continuing to speak of circuitry which enables selecting between "fast page pipeline and burst". The Applicant's representative was unable to find any portion of Manning to support the idea that fast page mode is the same as pipelined mode, and requests that the support for this proposition in the teachings of Manning (it is not to be found in col. 5, lines 43-50, which merely discuss the possible existence of a pipelined architecture, having no description whatsoever as to how switching between pipelined and burst modes might be accomplished) be designated with more specificity.

Second, the Office Action has failed to produce a *prima facie* case of anticipation. The only references offered to support the assertion that Manning "discloses the invention as claimed" with respect to claim 59 are: Figs.1 and 2, ADDR, ROW, and /WE; col. 5, lines 43-50;

col. 6, lines 14-26; and col 7, lines 43-54). Figs. 1 and 2 show a memory which may operate in burst or page modes (see col. 6, lines 14-16), and which may receive a row address. Col. 5, lines 43-50 discuss the possibility of using a pipelined architecture as an *alternative* to burst operation, but not as enabling switching between pipeline or burst operations within the *same* memory, "on-the-fly", as disclosed and claimed by the Applicant (see original application text, page 33, line 19). Col. 6, lines 14-16 merely confirm the ability to conduct burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Finally, col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Again, Manning gives no support whatever to the idea that a pipelined mode of operation is the same as a fast page mode. Thus, Manning never discusses the ability to *select, switch or choose* between burst and pipelined modes of operation, as claimed by the Applicant in independent claims 59, as well as in independent claims 36, 63, 65, 66, 67, 68, 69, 75, and 80, and all of the claims which depend from them.

Third, the Applicant cannot find where Manning discusses that these modes are interchangeable, or combinable, such that the term "fast page pipeline" proffered in the Office Action (in § 9) is defined. The Applicant fails to understand the meaning of this particular phrase, and looks to the Office for a more detailed explanation. Otherwise, the Office Action assertion that Manning discloses "selecting between a burst mode and pipeline modes of operations" is simply not supported by any of the teachings of Manning.

Fourth, the Applicant's representative has also reviewed the Rossini reference mentioned in the Office Action at § 9. It should be noted that Rossini issued on June 7, 1995, which is less than one year before the application from which the instant application was divided, was filed (U.S. Patent Ser. No. 08/650,719, still pending, was filed on May 20, 1996). The Applicant reserves the right to file a Petition under 37 C.F.R. § 1.131 to swear behind the Rossini reference, if necessary. It should also be noted that Rossini merely reveals the ability to use a cache controller with various SRAM types ("standard", "burst", or "pipelined burst"). Selecting between "burst and burst pipeline [modes of operation]" within the same memory, on-the-fly, is simply not disclosed, as asserted in the Office Action.

In short, what is discussed by Manning is not identical to the subject matter of the present invention as required by the M.P.E.P., and therefore, the rejection is improper. Reconsideration

and allowance of claims 36-39, 59-62, and 75-83 is therefore respectfully requested.

§103 Rejection of the Claims

Claims 63-69 were rejected in § 8 of the application under 35 USC § 103(a) as being unpatentable over Manning (U.S. Patent No. 5,610,864) in view of Ryan (U.S. Patent No. 5,966,724) or Rosich et al. (U.S. Patent No. 5,587,964). The Applicant respectfully traverses this rejection by the Office.

To establish a prima facie case of obviousness, the references themselves must provide a suggestion or motivation for combination. MPEP §2143.01. References must be considered in their entirety, including parts that teach away from the claims. MPEP 2141.02. "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed Cir., 1988). In this case, the devices taught in the references are not the same as that claimed by the Applicant, and can not be combined to operate as such. Further, each of the references fail to teach the element of *switching, selecting, or choosing* between pipelined and burst modes of operation. Finally, Manning and Ryan teach away from any such combination.

The Applicant is unable to find how Ryan or Rosich et al., in combination with each other, or with Manning, serve to teach the invention disclosed in claims 63-69. The Applicant has already discussed why Manning is defective as a reference (i.e., Manning fails to disclose *selecting, choosing, or switching* between burst and pipelined modes of operation). Even so, many assertions are made in the Office Action to the effect that Manning discloses switching or changing modes to a pipelined mode (even using a mode select signal, which is nowhere to be found in Manning - see § 8 of the Office Action, regarding claim 66), to the extent of specifying where in the cycles of a memory operation the change in modes occurs (see § 8 of the Office Action, regarding claims 66-67). However, the Applicant can find no such teaching in Manning, Ryan, or Rosich et al., each of which utterly fails to disclose *selecting, choosing, or switching* between burst and pipelined modes of operation. Thus, the Applicant looks to the examiner to provide more specific citations in the references, rather than continually referring to a single statement in Manning (col. 5, lines 43-50) which alludes to the possible existence of a pipelined architecture, having absolutely no description as to how such an implementation might be

accomplished - especially with regard to changing between operational modes (including a pipelined mode) at will, in the same memory, using individual operational signals.

As admitted in the Office Action, "Manning does not specifically disclose a step of changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state". This is because Manning fails to disclose any type of mode select signal for pipelined operation whatsoever.

Ryan teaches standard EDO, fast page mode EDO, and burst EDO modes of operation, without any showing of how one might switch to a pipelined access mode. Within the Ryan burst memory device, certain addresses can be *received* in a pipelined manner. However, Ryan does not switch between a burst and a pipelined mode of operation - instead, pipelined addresses may merely be received in the burst mode. This is fundamentally different from switching between burst and pipelined modes of operation. The Applicant can find no reference in the entire Ryan specification to support switching between burst and pipelined modes of operation. Instead, Ryan's device operates as a synchronous burst access memory device, as is clear from a reading of the Ryan disclosure. As no mention has been made in either reference of switching, selecting, or choosing between burst and pipelined modes of operation, combining the references does not result in both burst and pipelined modes of operation. It is only hindsight gained from the Applicant's disclosure which suggests having both burst and pipelined modes of operation in a memory, and switching therebetween.

Rosich et al. merely discloses switching between a page mode and a nibble mode. There is no discussion of a pipelined access mode by Rosich et al., whatsoever. Thus, the combination of Ryan and/or Rosich et al. with Manning does not cure the admitted primary defect of Manning, nor the defect of any of the cited references, to disclose switching between burst and pipelined modes of operation.

Further, it is improper to combine Ryan and Manning. Ryan teaches a synchronous memory device. *See* the Title and the Abstract of Ryan. As the Office notes, Manning discusses an asynchronous memory device. *See* for example, page 3 of the Office Action dated April 25, 2000. The M.P.E.P. requires that the asserted combination of the references must not render the prior art unsatisfactory for its intended purpose, or change the principle of operation of the reference being modified. *See* M.P.E.P. § 2143.01. One of ordinary skill in the art would not be

led to combine the dissimilar operation of these two references because doing so would clearly change the fundamental principle of operation for each device disclosed, rendering one or the other unfit for its intended purpose. In addition, it is improper to combine references where the references teach away from their combination. See M.P.E.P. § 2145(X)(D)(2). In this case, each reference teaches away from the other: Manning teaches asynchronous operation, while Ryan teaches synchronous operation.

Still further, although it is asserted that Ryan discloses the step of "changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state", the Office Action never states *which signals* in Ryan are to be used to select a pipelined mode of operation, and then to switch from pipeline to burst mode. Similarly, no specific mention is made as to *which signals* in Ryan are used to select the pipelined mode, and which signal is to be the enabling signal maintained in an active state. For example, although the "RAS" signal is noted in the Office Action, the Applicant can not see how this signal is used as an enabling signal during a pipelined mode operation, and requests a specific description as to how this might occur. Finally, as was noted in a previous response to the Office, it is a specific unaddressed problem of asynchronous DRAMs to switch between burst and pipelined modes of operation, since it was not previously needed (see Background of The Invention, page 5, lines 16-22). Ryan most certainly is not directed toward the solution of this problem.

Since the circuitry of Manning, Ryan, and Rosich et al. does not operate similarly to the Applicant's invention (i.e. switching between pipelined and burst operational modes is not disclosed or enabled) and a combination of the circuits would therefore be inoperative, since the cited references fail to teach all aspects of the Applicant's invention as claimed, since combining the references is improper, and since the references teach away from the combination asserted in the Office Action, the Applicant respectfully requests reconsideration of the rejection of claims 63-69 under 35 U.S.C. §103.

CONCLUSION

The Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Mark Muller, at (210) 308-5677 to facilitate prosecution of this application, including suggesting necessary amendments.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 16 day of October, 2001.

Name Tina Pugh

Signature _____